DC-20 GHz $N \times M$ Passive Switches

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Abstract — **High-order, bidirectional, dc-20 GHz switch networks have been developed. Single-chip 1×2, 1×4, and 2×2 switch MMIC's have been demonstrated. Multiple chips have been used to demonstrate 4×4 and 1×16 switches.**

The switches all use a combination of series and shunt passive FET switching elements. The 1×4 switch is made of a single stage of switching elements, rather than the usual two stages of 1×2 switches. The 2×2 switch is comprised of two stages of 1×2 switches. The multiple-chip 4×4 switch is made of four stages of 1×2 switches (using the 2×2 switch MMIC's). Two stages of 1×4 switches are used to make the 1×16 switch.

I. INTRODUCTION

BROAD-BAND MMIC switches using a combination of series and shunt passive FET switching elements have been demonstrated previously [1]–[3]. Most of these switches have been 1×2 circuits (also referred to as transmit/receive or single-pole double-throw switches). The highest order switch of this type has been a 2×2 switch (also referred to as a double-pole double-throw switch) [3]. Broad-band switches with active FET switching elements have also been demonstrated [4]. A multiple-chip MMIC 1×4 switch has been demonstrated using a combination of active and passive switching elements [5]. The switches presented in this paper are far smaller, are bidirectional, and have excellent switching speed. Unlike active switches, the switches presented in this paper require only gate bias and consume essentially no bias power.

The high-order switches presented in this paper all use passive FET switching elements. In a switching FET, no bias is applied between the source and the drain; only gate bias is used. In the "on" state the gate is biased at 0 V relative to the source and the drain. In the "off" state the gate is biased beyond pinch-off [6]. It has been shown that switching FET's may be sufficiently modeled as a resistance in the "on" state (R_{on}), and as a capacitance and a resistance in series in the "off" state (C_{off} and R_{off}) [2]. The switch FET states and models are summarized in Fig. 1, which includes typical values for the devices used in the switches presented in this paper.

II. 1×2 SWITCH STRUCTURE

The schematic of the 1×2 switch is shown in Fig. 2(a). This is a conventional broad-band circuit using a combination of series and shunt switching FET's. Fig. 2(b) shows the equivalent circuit for the 1×2 switch when it is biased to pass signals between ports RF1 and RF3 and to isolate

Manuscript received May 6, 1988; revised July 26, 1988.

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IEEE Log Number 8823763.

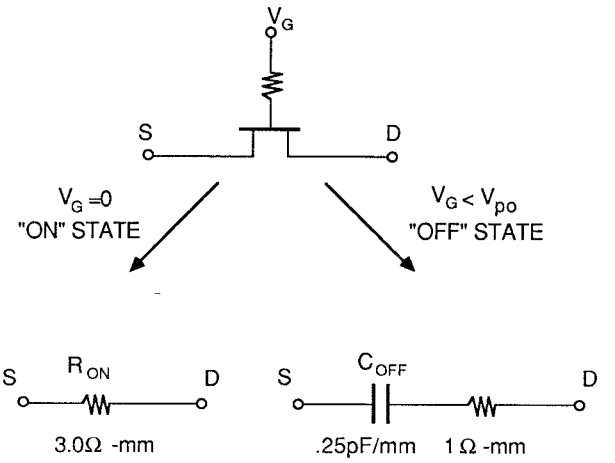

Fig. 1. Switch FET model.

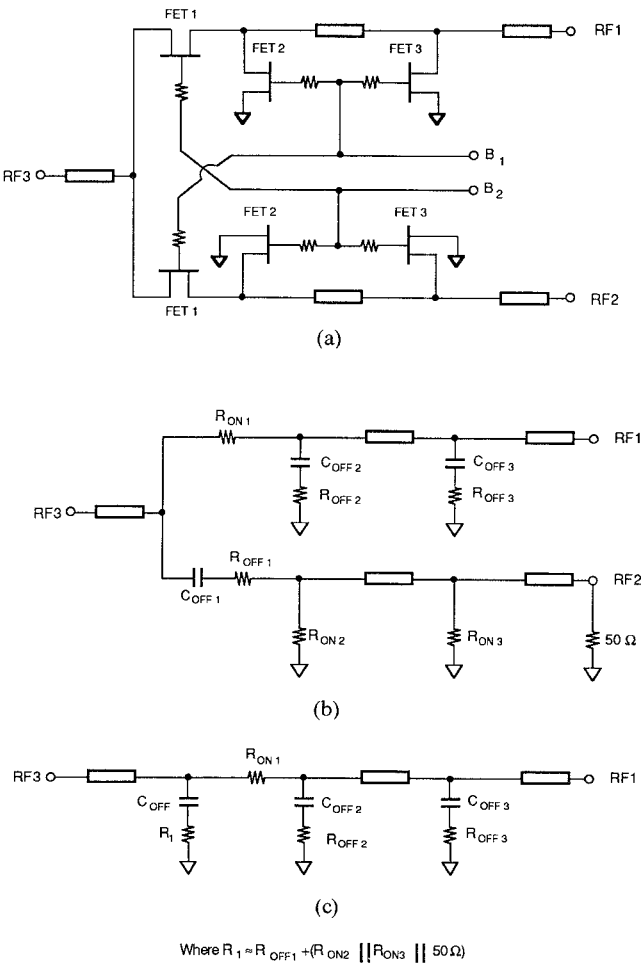

Fig. 2. (a) Schematic of the 1×2 switch. (b) Equivalent circuit. (c) Simplified equivalent circuit.

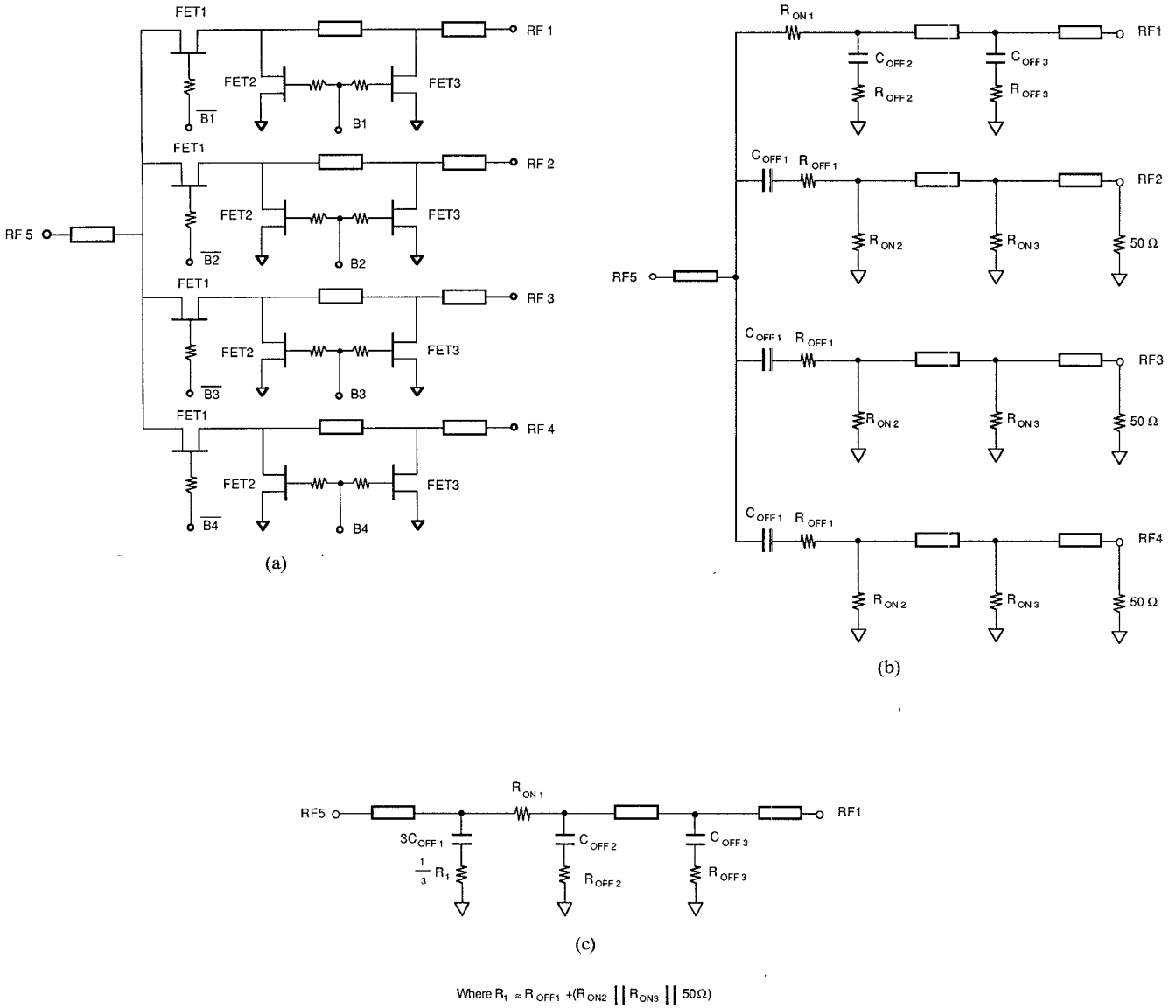

Fig. 3. (a) Schematic of the single-stage 1×4 switch. (b) Equivalent circuit. (c) Simplified equivalent circuit.

between ports RF2 and RF3. At low frequencies the series FET provides adequate isolation. At high frequencies, where C_{off} is significant, however, isolation is primarily provided by the low resistances of R_{on2} and R_{on3}.

The loss mechanisms between RF1 and RF3 are more clearly seen in the simplified equivalent circuit in Fig. 2(c). A portion of the loss (the dc loss) is contributed by the series FET (R_{on1}). Insight into the other major loss mechanism is gained by viewing the circuit in Fig. 2(c) as an artificial transmission line. At high frequencies the loss through the shunt elements (C_{off1} and R_1, C_{off2} and R_{off2}, and C_{off3} and R_{off3}) is also significant, similar to the attenuation in the gate line of a distributed amplifier [2]. Note that the various resistive elements in the RF2 arm can be adequately modeled as a single resistance, R_1. Mismatch losses can also become significant at high frequencies if the shunt capacitances (C_{off1}, C_{off2}, and C_{off3}) are excessive.

III. 1×4 Switch Structure

The schematic of the single-stage 1×4 switch is shown in Fig. 3(a). The structure is similar to the 1×2 switch, but with four series FET's (FET1) tied to a common node rather than two. Each series FET is followed by two shunt FET's. The equivalent circuit of the 1×4 switch is shown in Fig. 3(b) for the state in which signals are passed between RF1 and RF5, and all the other ports are isolated (RF2, RF3, and RF4). Like the 1×2 switch, low-frequency isolation is provided by the "off" capacitance of the series FET's (C_{off1}) and at higher frequencies by the "on" resistance of the shunt FET's (R_{on2} and R_{on3}).

The principal insertion loss components of the 1×4 switch are evident in the simplified equivalent circuit in Fig. 3(c). Like the 1×2 switch, the primary dc loss component comes from the "on" resistance of the series FET (R_{on1}). Additional high-frequency loss components are

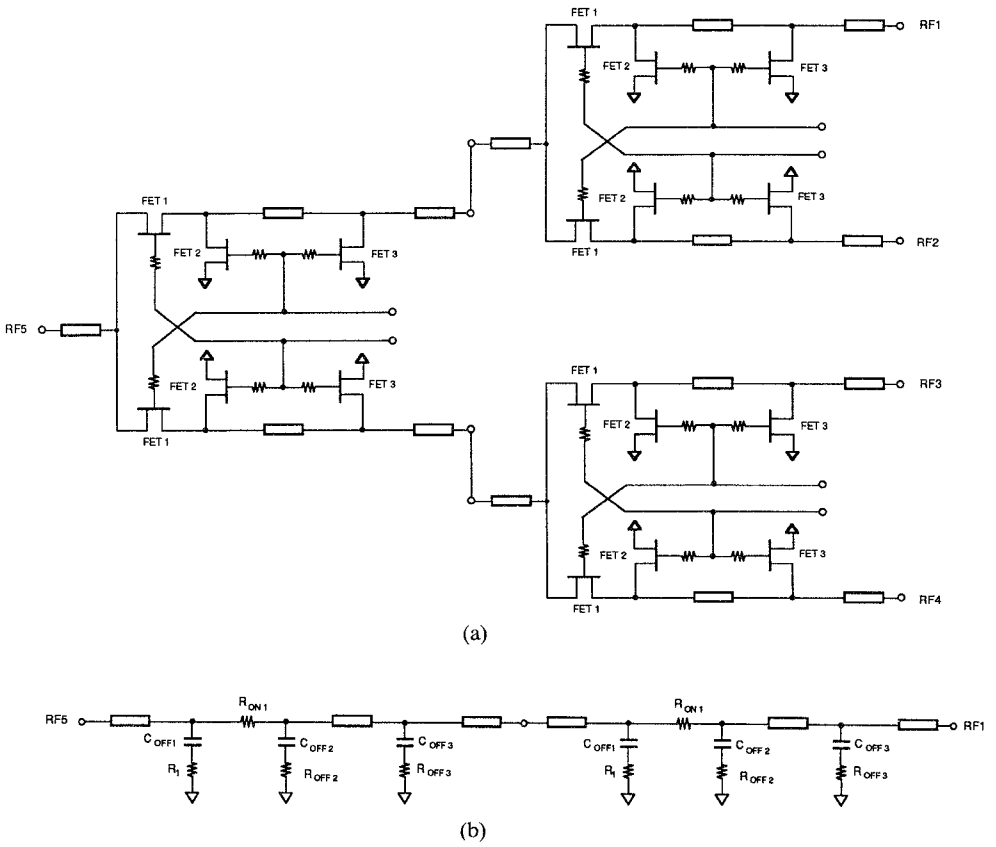

Fig. 4. (a) Schematic of conventional two-stage 1×4 switch. (b) Simplified equivalent circuit.

contributed by the shunt elements ($3C_{off1}$ and $R_1/3$, C_{off2} and R_{off2}, and C_{offf3} and R_{off3}). Note that the first shunt element is different than it is in the 1×2 switch, consisting of three times the capacitance ($3C_{off1}$) and one third the resistance ($R_1/3$). The higher capacitance can lead to much higher losses, but this is partially offset by the reduced resistance. The higher capacitance also leads to higher mismatch losses. In circuit implementations, the periphery of FET1 is reduced in the 1×4 switch (relative to the 1×2 switch) in order to reduce C_{off1}. A higher dc loss component results (from R_{on1}), but this is more than offset by the reduction in losses at the high end caused by C_{off1}.

Fig. 4(a) shows a more conventional 1×4 switch structure, realized with two stages of 1×2 switches. This switch structure is shown for comparison only, and has not been demonstrated. The losses of this type of 1×4 switch are evident in the simplified equivalent circuit in Fig. 4(b). This is simply two of the 1×2 equivalent circuits from Figs. 2(c) in cascade. The loss of the two-stage switch comprises two dc series resistances (R_{on1}'s) and the capacitive shunt loss elements of two stages. The two-stage 1×4 switch in Fig. 4 has more loss-contributing elements than the single-stage 1×4 switch in Fig. 3. This can more than offset the higher loss of some of the individual elements in the single-stage 1×4 switch (such as R_{on1}). A single-stage 1×4 switch can therefore have significantly lower loss than a two-stage 1×4 switch.

Besides lower loss, the single-stage 1×4 switch configuration has other advantages. The total MMIC real estate required is much smaller for the single-stage 1×4 switch. In order to connect all four series FET's (FET1's), a tight layout is required, but as is demonstrated by the results below, 30 dB isolation can still be achieved.

The isolations of the single-stage 1×4 and of the two-stage 1×4 switches are comparable. Worst-case isolation for the two-stage 1×4 switch is the same as for a single 1×2 stage. For example, when the switch in Fig. 4 is biased to pass signals between RF1 and RF5, the isolation between RF2 and RF5 is the same as for a single-stage 1×2 switch. Thus the isolations of the one-stage and two-stage 1×4 switches are comparable. Note that isolation may readily be improved by adding more shunt switching elements. Much higher isolation can be achieved, with only small increases in insertion loss.

IV. Higher Order Switch Structures

The schematic of the 2×2 MMIC switch is shown in Fig. 5. This switch is made up of four 1×2 switches in a two-stage cascade. One RF crossover is used. The performance of this switch is closely related to the 1×2 switch in Fig. 2. Since there are two stages, insertion loss is double. Ideally the isolation is also doubled, but as a practical matter it is reduced by proximity effects in the layout and by coupling across the RF crossover. A 4×4 switch can be made of four of the 2×2 switch MMIC's, as is shown in

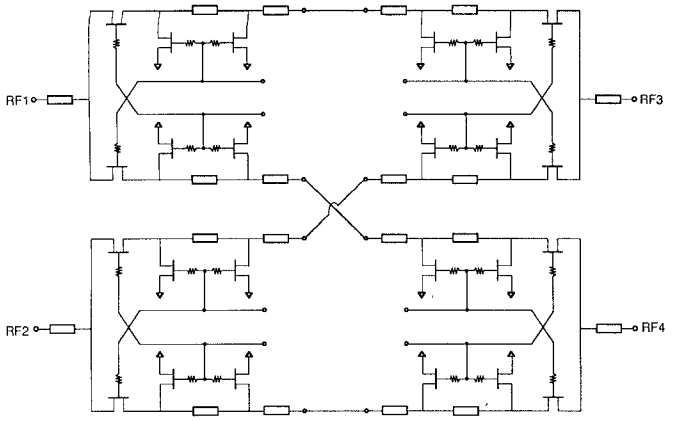

Fig. 5. Schematic of the 2×2 switch.

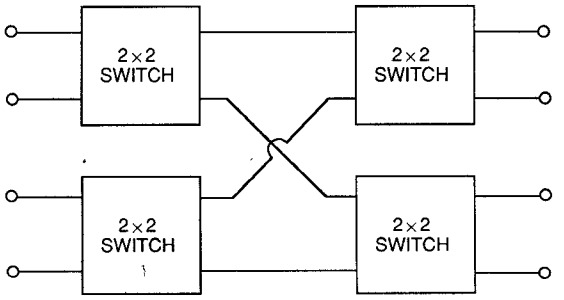

Fig. 6. Diagram of the 4×4 switch.

Fig. 6. This configuration imposes only one additional RF crossover (other crossovers are within the 2×2 switches).

A 1×16 switch has also been assembled. It comprises two stages of the 1×4 switch. Its performance is therefore closely related to the performance of the 1×4 switch. Insertion loss is expected to double. Isolation will increase only between RF ports not on the same 1×4 switch MMIC.

V. MMIC Layout and Fabrication

The 1×2, 2×2, and 1×4 switches were all fabricated as single-chip MMIC's. Ion implantation was used to realize an active layer carrier concentration of $1.8 \times 10^{17}\,\mathrm{cm}^{-3}$ and a contact layer concentration of $1 \times 10^{18}\ \mathrm{cm}^{-3}$. A gate recess is used, resulting in an I_{dss} of 350 mA/mm and a pinch-off voltage of −3.5 V. The gates have a length of 0.5 μm and were E-beam defined. All resistors are 2 kΩ and are made with multiple open-gate FET's in series. The entire wafer is passivated with silicon nitride. No capacitors are used. The wafer has been thinned to 4 mils, and 20×100 μm slot via holes have been plasma etched.

The complete 1×2 MMIC is shown in Fig. 7. The chip measures only 35×45 mils (0.89×1.14 mm). A compact layout is used with all the FET's in the same orientation. RF1 and RF2 are separated as much as possible for maximum isolation and for ease of use. Each FET is individually biased directly through a 2 kΩ resistor to ensure maximum switching speed.

The complete single-stage 1×4 switch is shown in Fig. 8. This chip is only 50×55 mils (1.27×1.40 mm), only 75 percent larger than the 1×2 switch. Three of the 1×2 switches would be required to perform the functions of the 1×4 switch. The series FET's (FET1's) share a common node (connecting to RF5). The four shunt FET arms spread out from that point. Note that the orientations of the RF1 and RF4 arms are perpendicular to the orientations of the RF2 and RF3 arms. This does not lead to significantly different FET performance. Despite the proximity of the components of the various shunt arms (RF2 and RF3 in particular), adequate isolation was achieved.

The complete 2×2 MMIC switch is shown in Fig. 9. Note that there are some dc test structures in the top center of the chip; these have no RF effect. It can be seen that the 2×2 switch is composed of four of the 1×2 switches in Fig. 7. This chip is only 70×80 mils (1.78×2.03 mm), slightly less than four times the size of the 1×2 switch. A single crossover is used. It would be possible to layout such a switch with no crossovers, but then RF1 and RF2 would not be on the same side of the chip, which would be inconvenient in end use. The crossover is only 10×10 μm so that coupling is minimized, and high isolation is maintained. This chip has a total of eight bias connections, but has only two states (RF1 connected to RF3 while RF2 connected to RF4, and RF1 connected to RF4 while RF2 connected to RF3). The biases could have been connected on chip, reducing the number of 2. It was decided to leave the biases separate since the ability to independently bias each switch allows for more thorough diagnosis of the switch's performance. Now that adequate performance has been demonstrated, biases will be connected on chip.

VI. Measured Performance of Single-Chip Switches

Measurements were performed on the three single-chip switches: 1×2, 1×4, and 2×2. Small-signal performance was measured for all of these switches. In addition, power performance and switching speed were measured on the 1×2 switch.

The power-handling and switching speed performance of the 1×2 switch is closely related to that of the other switches. The switching speed and power handling of the 2×2 and 4×4 switches can be inferred directly from measurements on the 1×2, since both of these switches are composed of multiple 1×2's. The switching speed and power-handling performance of the 1×4 and 1×16 can also be inferred from the 1×2 switch. Power handling on these switches is limited by current saturation through the series FET's in the "on" state. Since the series FET in the 1×4 is 65 percent smaller than in the 1×2, power handling may be reduced by as much as 4 dB. Switching speed is determined by the *RC* time constant of the bias resistor and the gate capacitance. Since the largest FET's in the 1×2 and the 1×4 switches are approximately the same size and the same value resistors are used, switching speed will be the same.

The small-signal performance of the 1×2 switch is shown in Fig. 10. Insertion loss is less than 2 dB to 20 GHz,

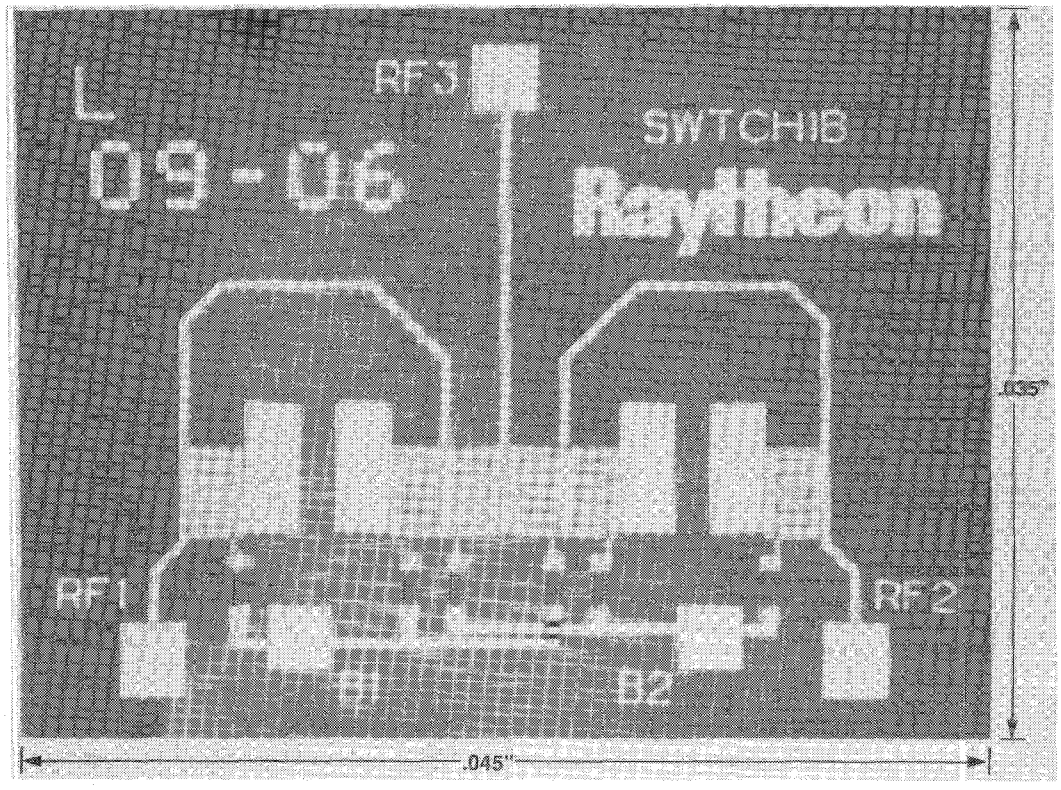

Fig. 7. Photograph of the 1×2 switch.

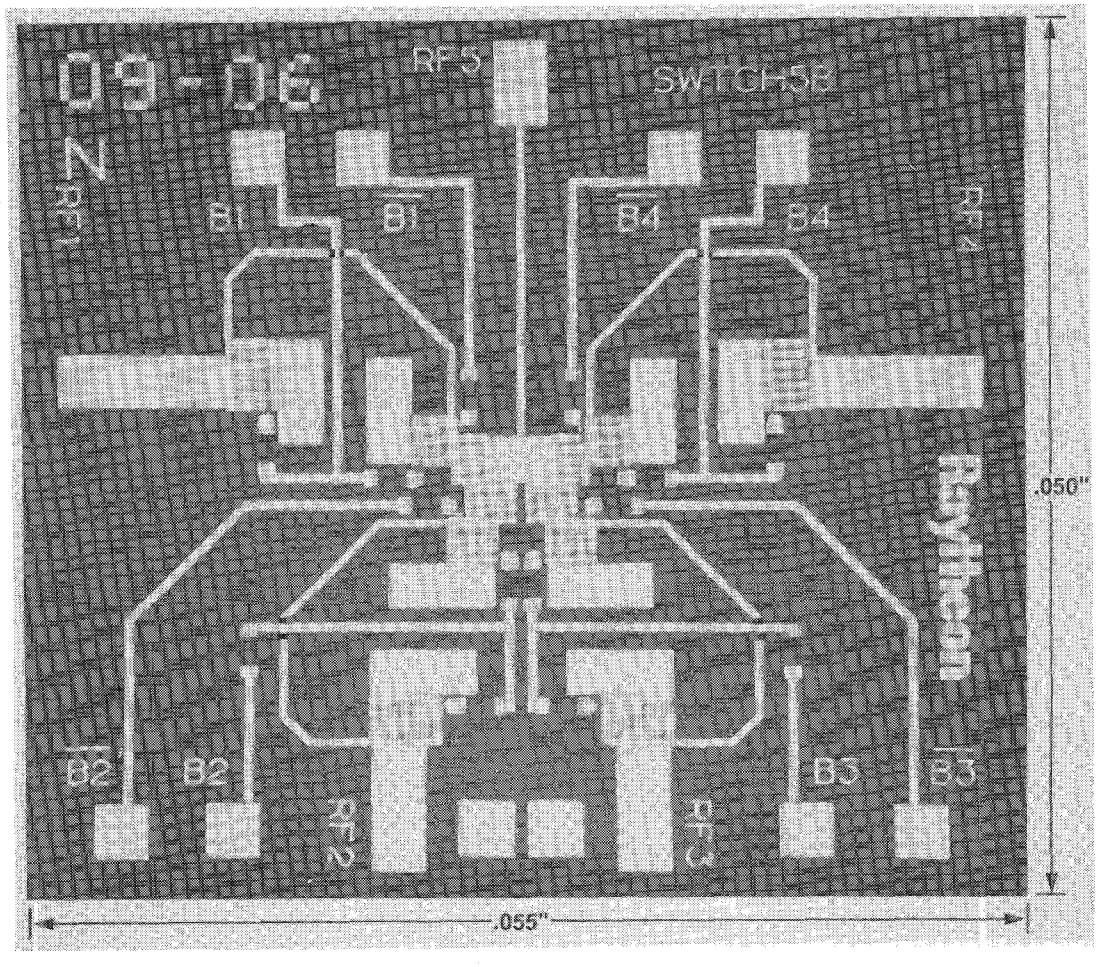

Fig. 8. Photograph of the 1×4 switch.

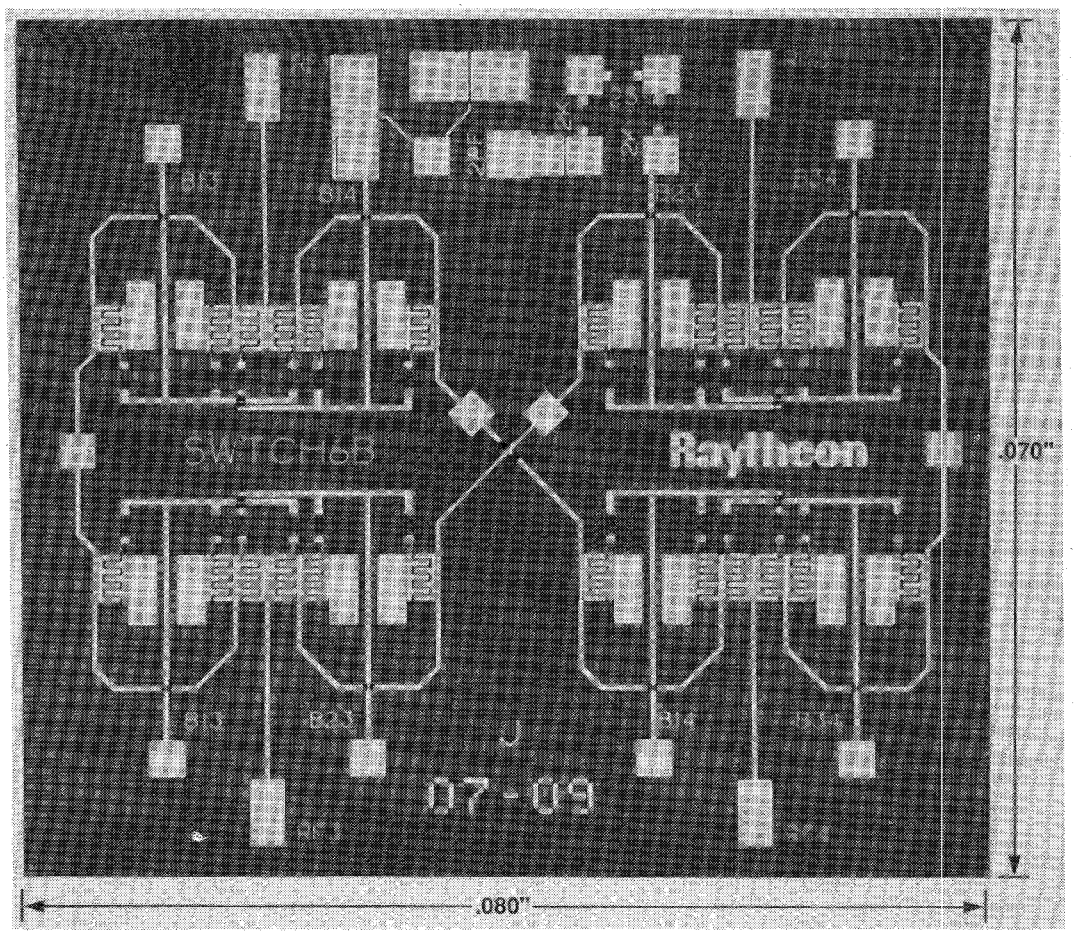

Fig. 9. Photograph of the 2×2 switch.

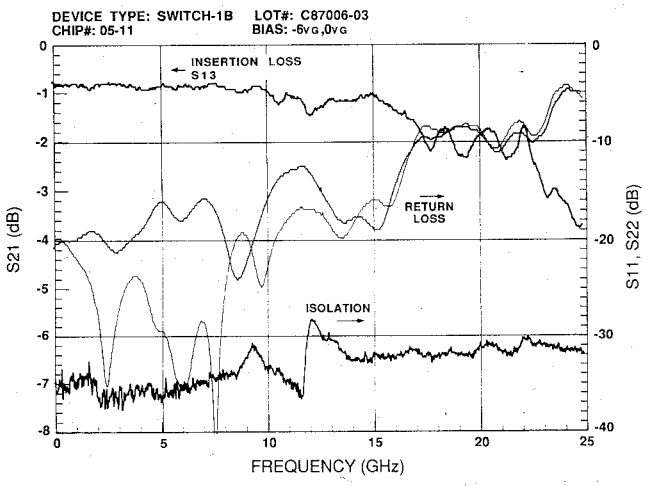

Fig. 10. Small-signal performance of the 1×2 switch.

isolation is better than 30 dB, and return loss is better than 10 dB. These data have been corrected for fixture loss. The effects of bond wires and fixture discontinuities have not been removed, however. Actual insertion loss and return loss can be expected to be somewhat better than the measurements show.

The power handling of the 1×2 switch is shown in Fig. 11. These are insertion loss power transfer curves taken at various frequencies up to 18 GHz. An ideal response is a

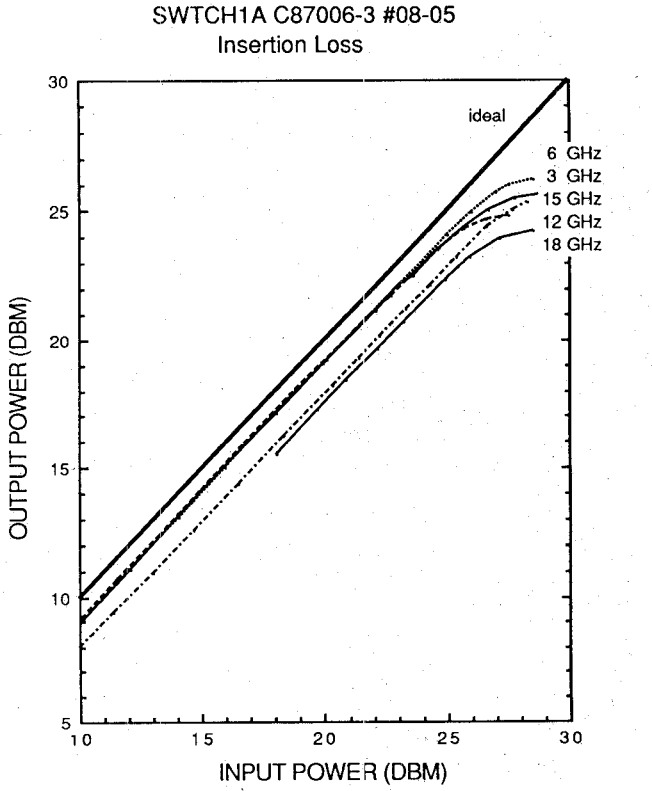

Fig. 11. Power handling for the 1×2 switch. Insertion loss power transfer curves are shown.

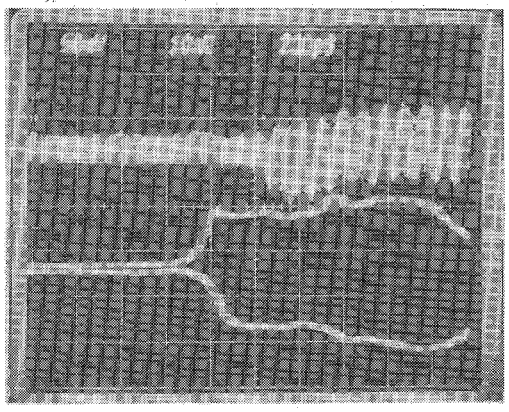

Fig. 12. Switching speed of the 1×2 switch. Top trace shows RF signal; bottom traces show bias signals.

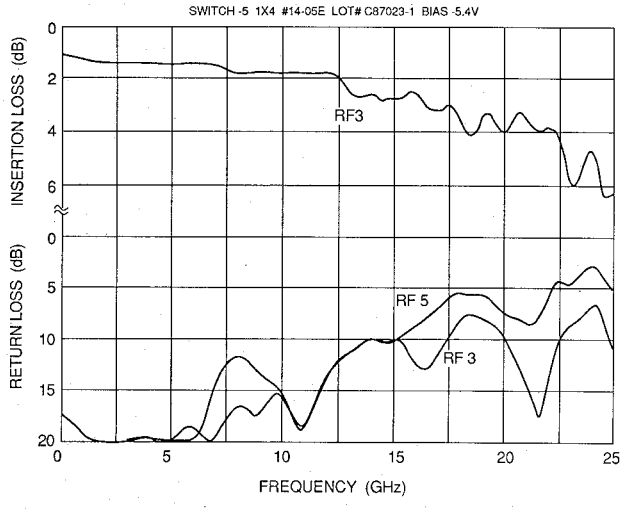

Fig. 13. Representative insertion loss and return loss of the 1×4 switch.

straight line with a slope of 1. The curves do not show signs of significant compression until 25 dBm (320 mW). 1 dB compression occurs at 27 dBm (500 mW). Isolation has also been measured over power. Up to 25 dBm (320 mW), isolation does not change measurably; up to 27 dBm, the change is less than 1 dB.

The switching speed of the 1×2 switch is shown in Fig. 12. The top trace shows the amplitude of a 10 GHz signal being passed through the switch. The lower traces are the complementary bias inputs to the switch. The turn-on time is better than 400 ps. The turn-off time (not shown) is similar to the turn-on time.

Representative performance of the single-stage 1×4 switch is shown in Figs. 13 and 14. Fig. 13 shows the insertion loss and return loss when the switch is biased to pass signals between ports RF3 and RF5. The performance of the other three states is not significantly different. Insertion loss is better than 2 dB to 12.5 GHz and better than 4 dB to 22 GHz. Return loss is better than 10 dB to 22 GHz, with the exception of two peaks to 8 dB between 15 and 20 GHz at the RF1, RF2, RF3, and RF4 ports; it is slightly worse at the RF5 port. Fig. 14 shows the isolation between port RF5 and ports RF1, RF2, and

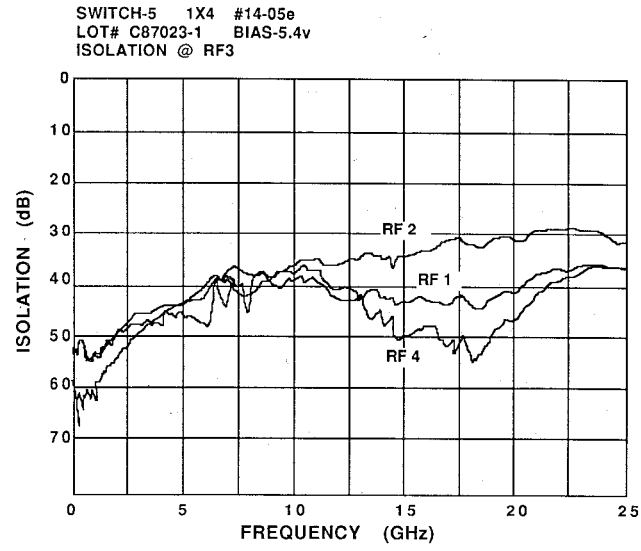

Fig. 14. Representative isolations of the 1×4 switch.

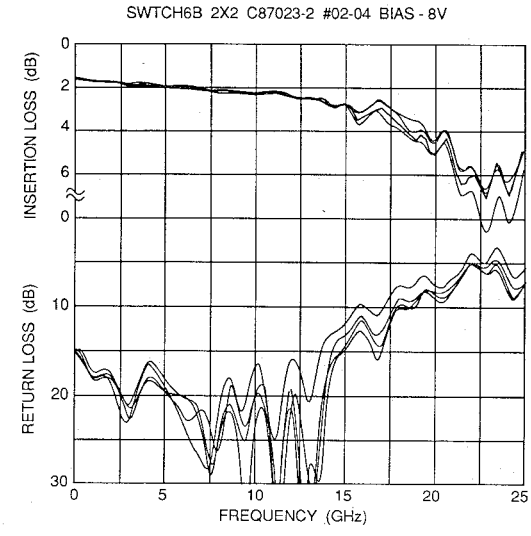

Fig. 15. Insertion losses and return losses for the 2×2 switch.

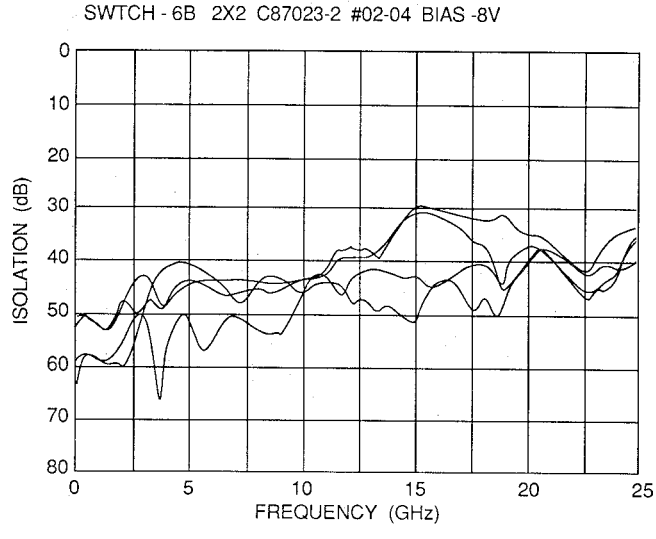

Fig. 16. Isolations for the 2×2 switch.

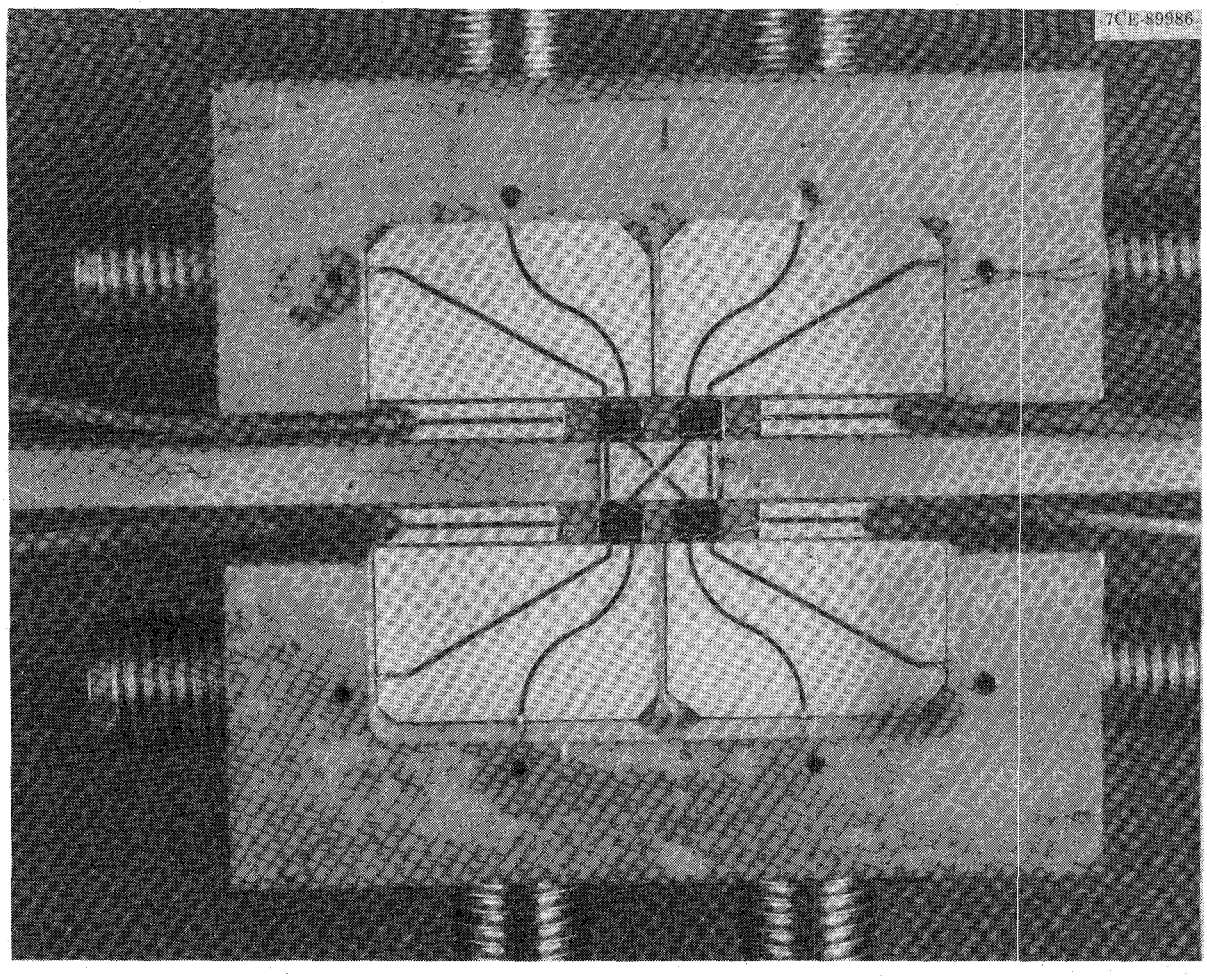

Fig. 17. Photograph of the 4×4 switch.

RF4 when the switch is biased to pass signals between RF5 and RF3. Isolation in other states is not significantly different. Isolation is better than 30 dB at port 3 and better than 38 dB to ports 1 and 4. The measurements on the 1×4 switch have been corrected for fixture loss but not for fixturing discontinuities or bond wire effects. The performance of the single-stage 1×4 switch is superior to what would be expected of a conventional two-stage 1×4 switch. Further, the single stage 1×4 switch has less total circuit complexity, and a far smaller chip size.

The performance of the 2×2 MMIC switch is indicated in Figs. 15 and 16. Insertion losses are less than 4 dB to 18 GHz, with a variation of less than 1 dB. The return losses are better than 10 dB to 17 GHz, with a worst-case return loss of 7 dB to 20 GHz. There are two sets of measured isolations, as can be seen in Fig. 16. When signals are not passed through the central crossover (from RF1 to RF3 or from RF2 to RF4), isolation is better than 40 dB to 25 GHz. Each of the component 1×2 switches have 30 dB isolation; thus 60 dB isolation may be expected. However, proximity effects on a single chip limit isolation to 40 dB. When signals are passed through the crossover (RF1 to RF4 or RF2 to RF3), isolation is better than 30 dB to 25 GHz. Coupling across the crossover therefore limits the isolation to 30 dB.

VII. Measured Performance of Multiple-Chip Switches

A 4×4 switch has been assembled of four 2×2 MMIC's, and is shown in Fig. 17. This switch has four separate states and requires a total of four bias lines. The performance for this switch is shown in Figs. 18, 19, and 20. As is expected, this performance is very closely related to the 2×2 switch's performance. Insertion loss for all 16 possible signal paths is shown in Fig. 18. The loss is less than 7 dB to 18 GHz, and the losses in all paths are within 1 dB of one another except for a small band about 15 GHz, where the variation is 2 dB. Representative isolations are shown in Fig. 19. The worst-case isolation is 30 dB to 12 GHz and degrades to 27 dB at 18 GHz. These isolations are fixture limited. Best-case isolations are greater than 40 dB to 25 GHz. Representative return losses are shown in Fig. 20. All return losses are better than 10 dB to 15 GHz, with states degrading to 7 dB at 18 GHz.

A 1×16 switch has been assembled of five 1×4 MMIC's, and is shown in Fig. 21. This switch has 16 different states, and because of the one-stage configuration of the 1×4's and the complementary bias requirements, a total of 16 bias lines are required. The performance for the 1×16 switch is shown in Figs. 22 and 23. As is expected, the

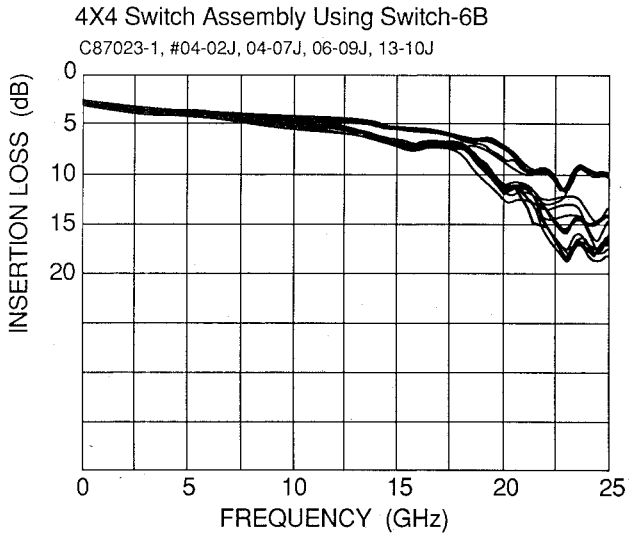

Fig. 18. All insertion losses for the 4×4 switch.

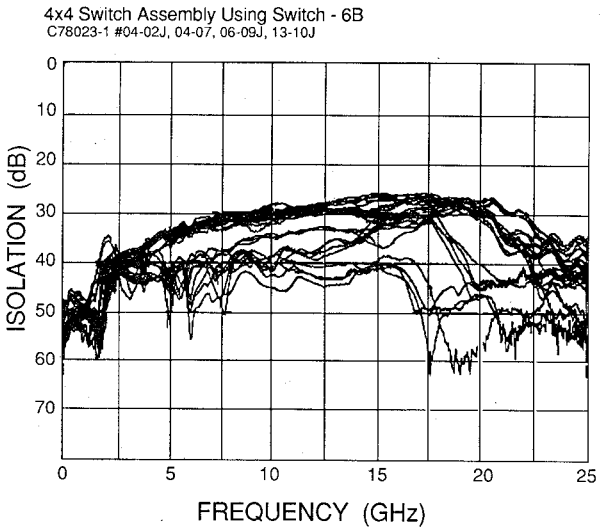

Fig. 19. Representative isolations for the 4×4 switch.

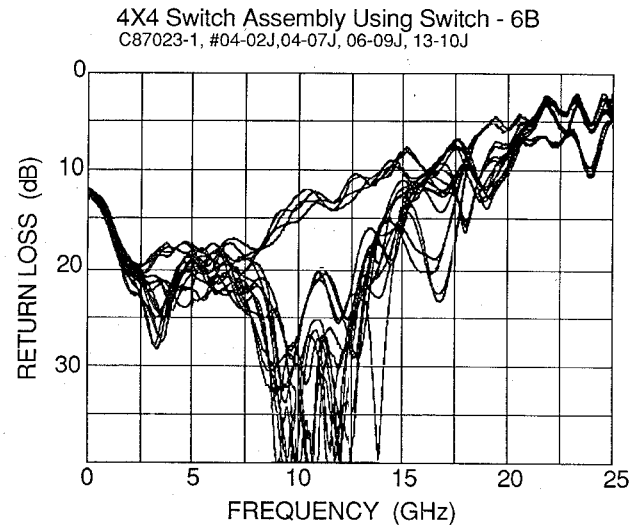

Fig. 20. Representative return losses for the 4×4 switch.

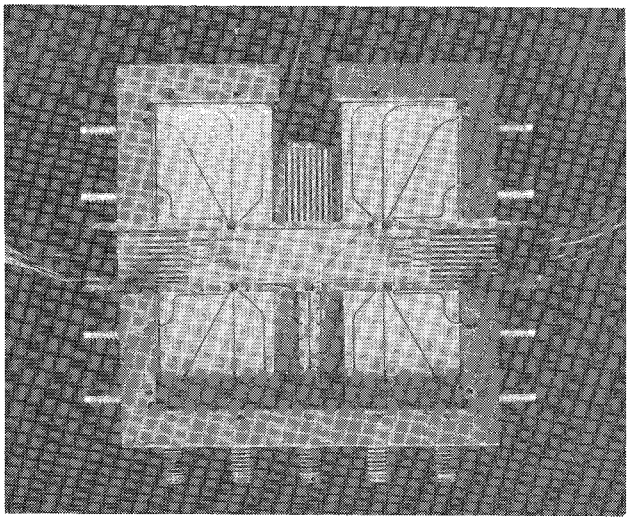

Fig. 21. Photograph of the 1×16 switch.

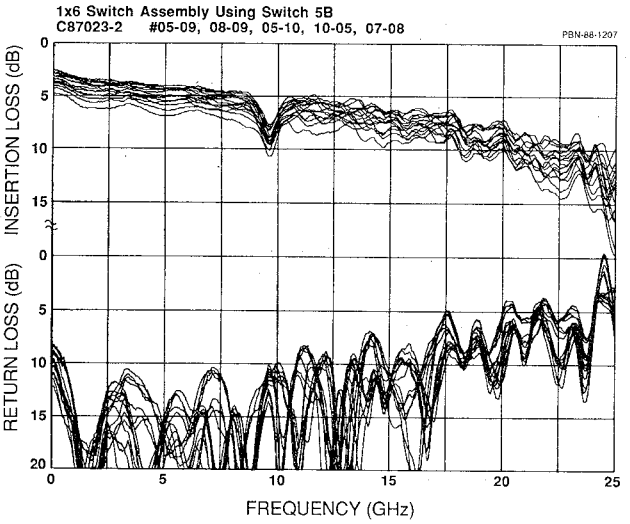

Fig. 22. All insertion losses and return losses for the 1×16 switch.

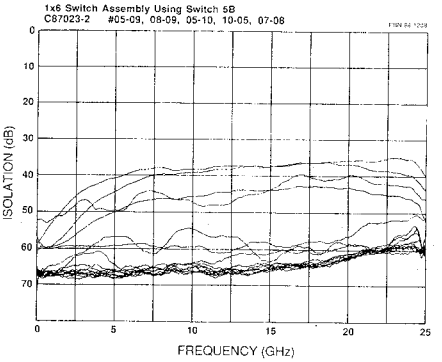

Fig. 23. Representative isolations for the 1×16 switch.

performance is very closely related to the 1×4 switch's performance. All 16 insertion losses and return losses are shown in Fig. 22. The losses are less than 8 dB to 18 GHz and less than 10 dB to 20 GHz. The losses have a moderate peak at 9 GHz, caused by a resonance in the alumina lines in the fixture. The loss varies by as much as 3 dB, depending on the signal path. The losses are somewhat

more than twice that of the 1×4 switch because of the long transmission line runs in the assembly. The return losses are very similar to that of the 1×4 switch, better than 10 dB to 13 GHz and degrading to 5 dB at 20 GHz. Representative isolations are shown in Fig. 23. Isolation is better than 35 dB to 25 GHz in all cases. The highest isolations in Fig. 23 are beyond the 65 dB isolation resolution limit of the equipment used, and are therefore actually better than indicated.

VIII. Summary

A series of dc–20 GHz MMIC component switches has been demonstrated, including 1×2, 1×4, and 2×2 single-chip switches. These MMIC's are the highest order single-chip switches demonstrated to date, and offer excellent performance. Loss increases with the complexity of the switch. It is less than 2 dB for the 1×2 switch, 4 dB for the single-stage 1×4, and 4 dB for the 2×2. Isolation is better than 30 dB for all switches. Switching speed is considerably less than 0.4 ns for all the switches. Power handling has been shown to be better than 25 dBm for the 1×2 and 2×2 switches, and is expected to be better than 21 dBm for the 1×4 switch.

The MMIC component switches have been used to realize higher order switches: a 4×4 switch comprising four 2×2 MMIC's and a 1×16 switch comprising five 1×4 MMIC's. These are the highest order MMIC based switches demonstrated to date. The performance of these switches is closely related to the MMIC's of which they are assembled. The component MMIC's can be used to realize a variety of other high-order switches.

Acknowledgment

The authors would like to thank D. Kelly for fixture design, fabrication coordination, and switch evaluation; R. Binder and D. Satterthwaite for testing; P. Hindle for process coordination; and J. Descoteaux and C. Engel for assembly.

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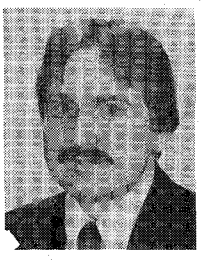

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Mary Ellen Miller was born in Boston, MA, in 1961. She received the B.A. degree in chemistry from Regis College, Weston, MA, in 1983.

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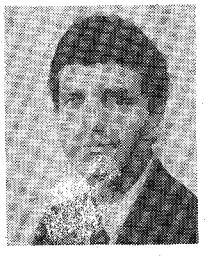

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